FIG. 1

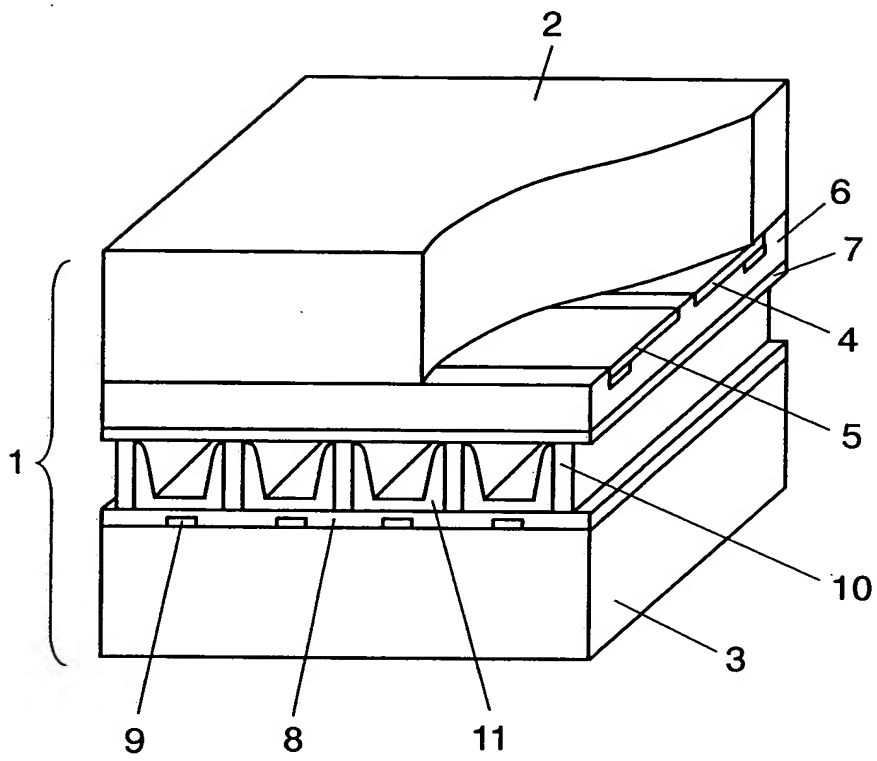


FIG. 2

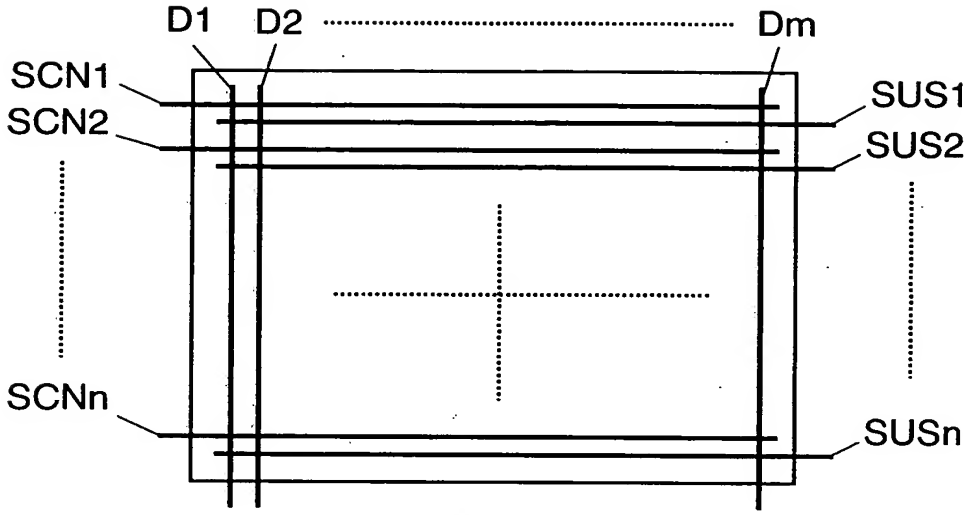


FIG. 3

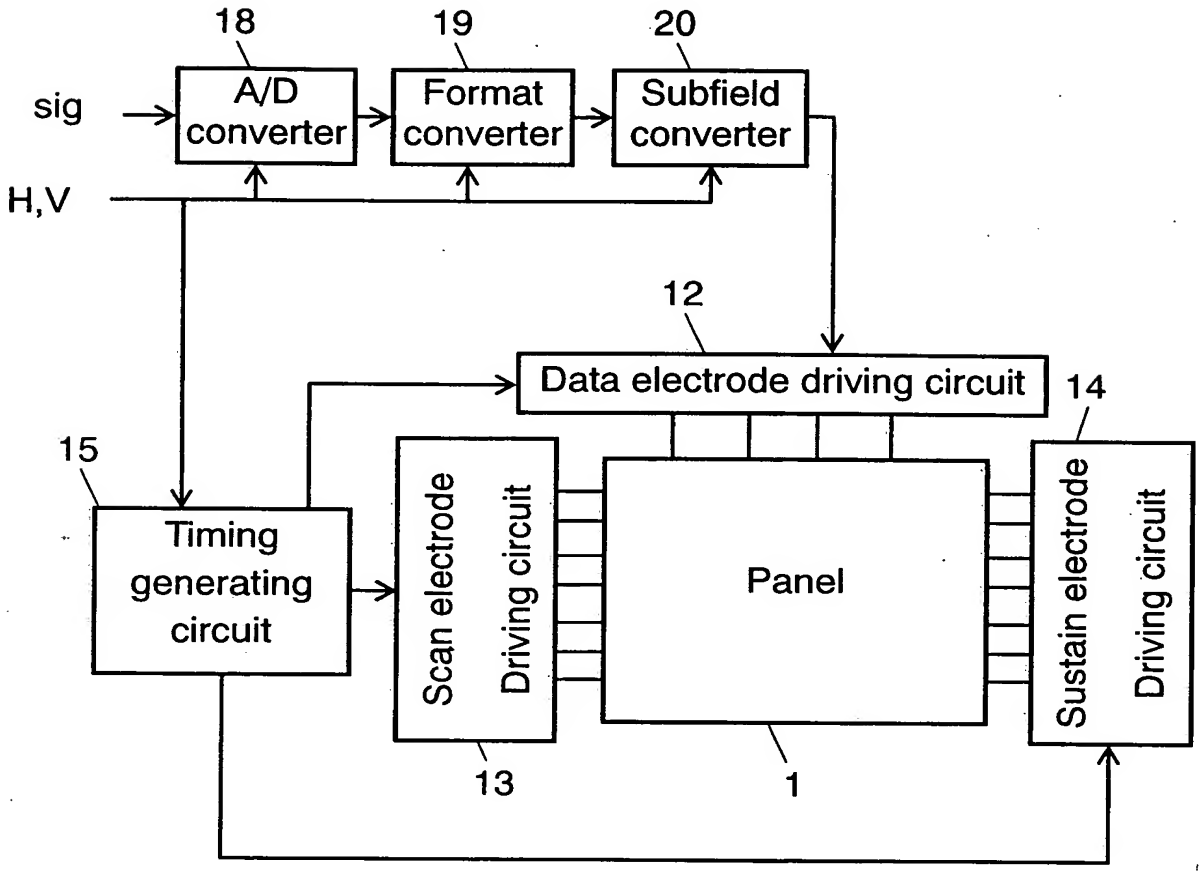
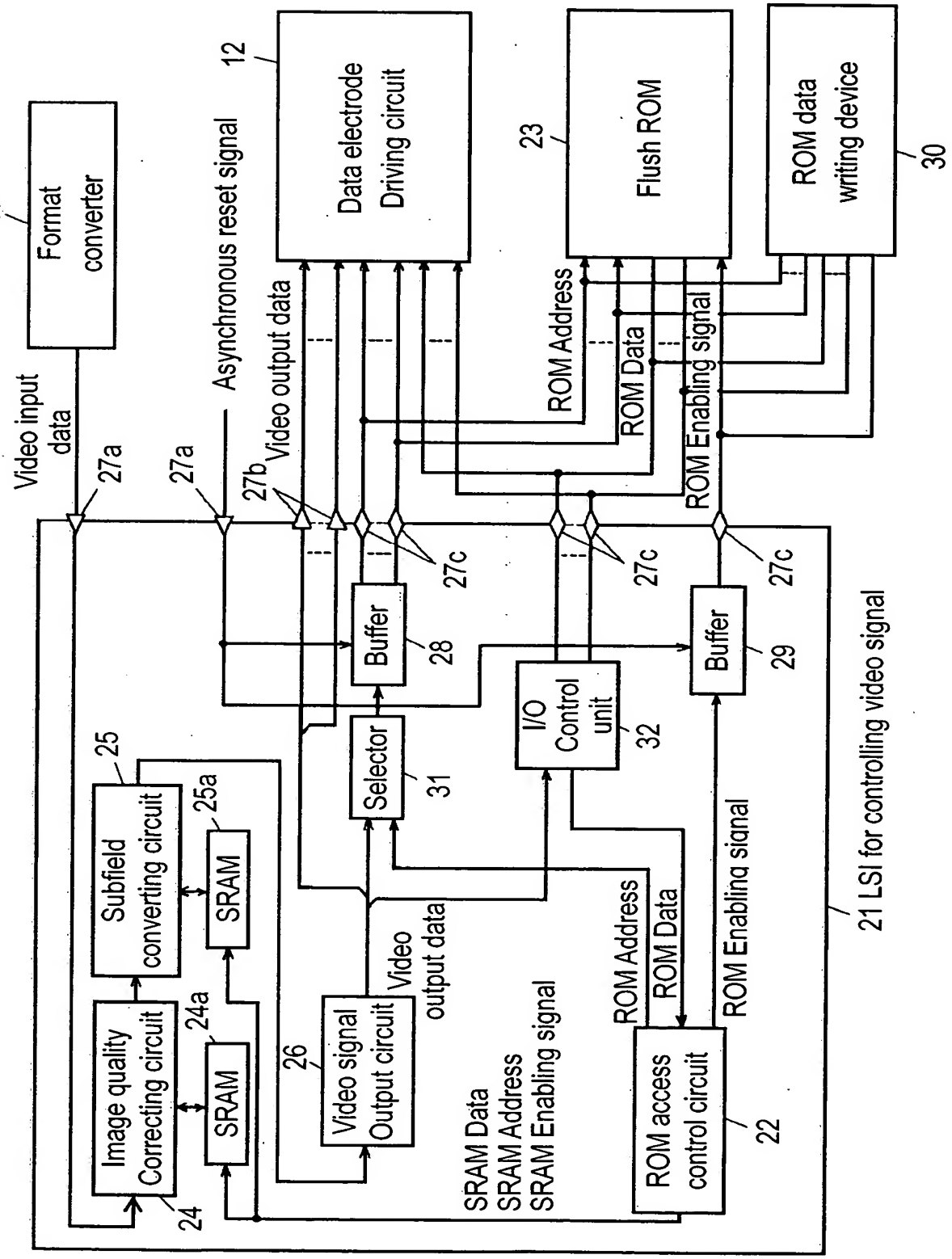

18
19
20
sig
A/D converter
Format converter
Subfield converter
H,V
12
Data electrode driving circuit
14
15
Timing generating circuit
Scan electrode Driving circuit
Panel
Sustain electrode Driving circuit
13
1

FIG. 4


19
Format converter
Video input data
27a
27a
Asynchronous reset signal
27b
Video output data
12
Data electrode Driving circuit
23
Flush ROM
ROM data writing device
30
ROM Address
ROM Data
ROM Enabling signal
27c
27c
27c
Buffer
28
Buffer
29
I/O Control unit
32
Selector
31
25
Subfield converting circuit
25a
SRAM
24a
SRAM
Image quality Correcting circuit
24
26
Video signal Output circuit
Video output data
SRAM Data
SRAM Address
SRAM Enabling signal
ROM Address
ROM Data
ROM Enabling signal
ROM access control circuit
22
21 LSI for controlling video signal

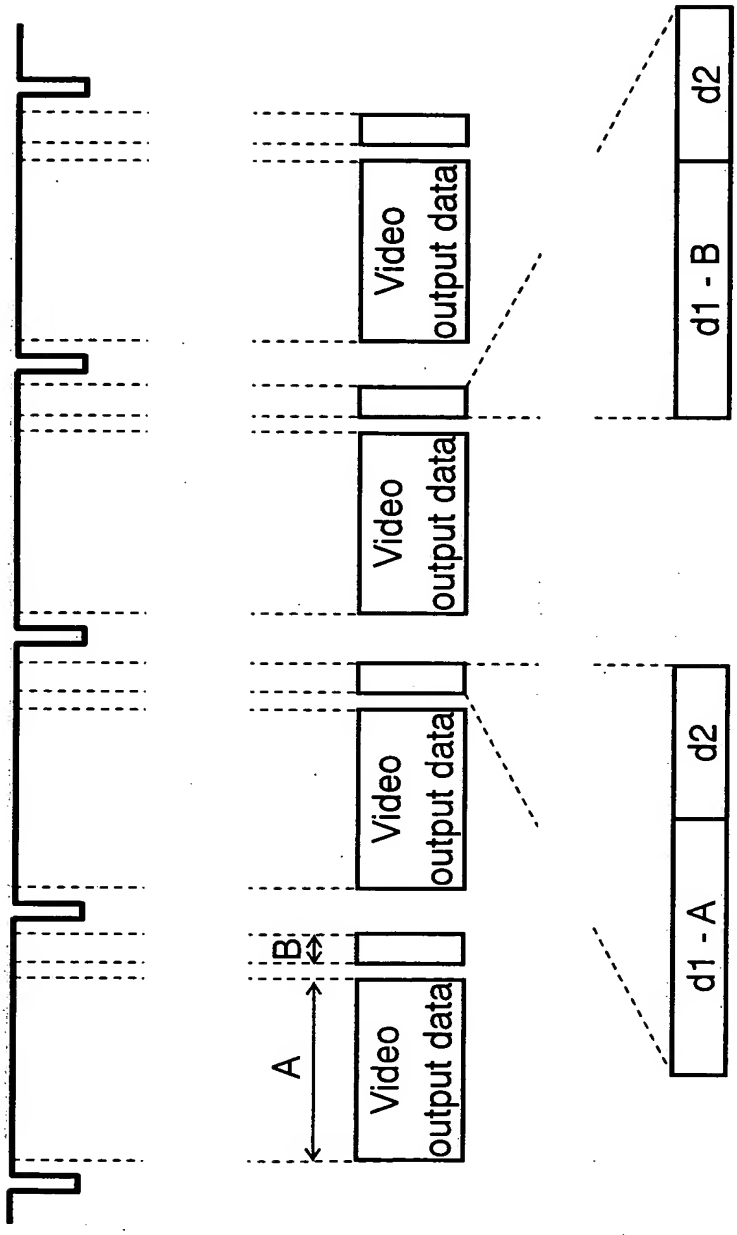


FIG. 5A

FIG. 5B

FIG. 5C

FIG. 6A

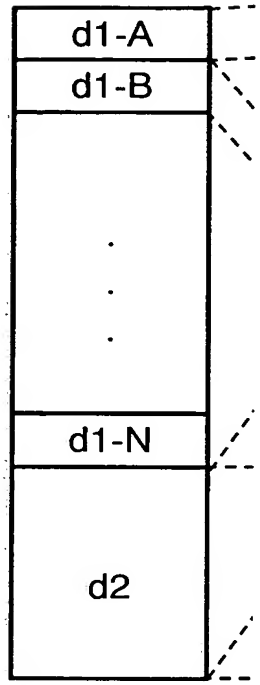


FIG. 6B

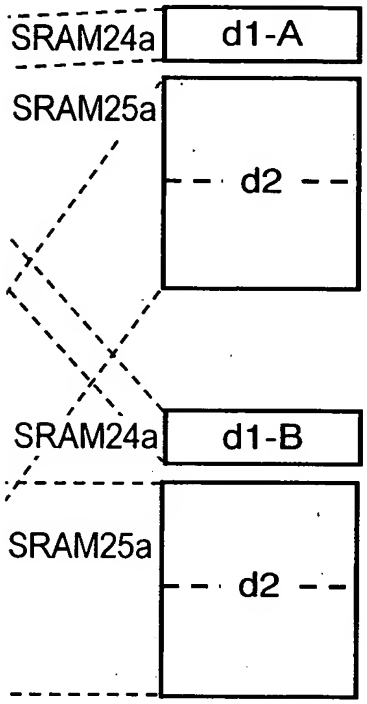


FIG. 6C

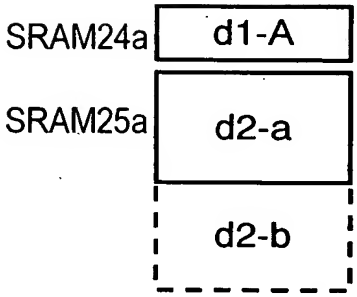


FIG. 6D

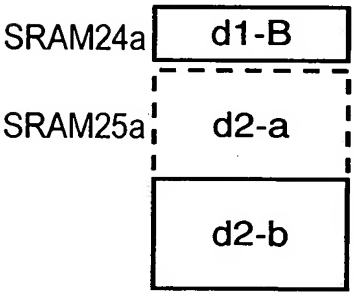


FIG. 7A

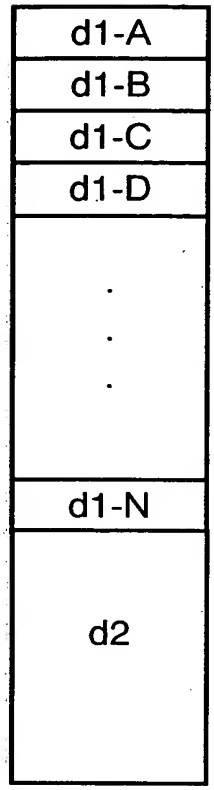


FIG. 7B

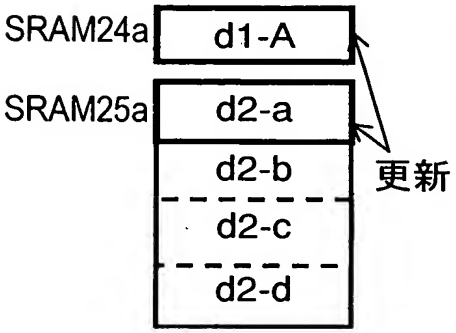


FIG. 7C

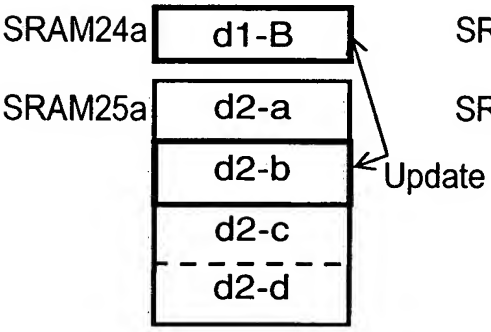


FIG. 7D

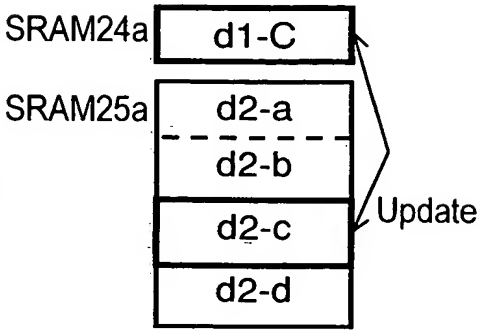
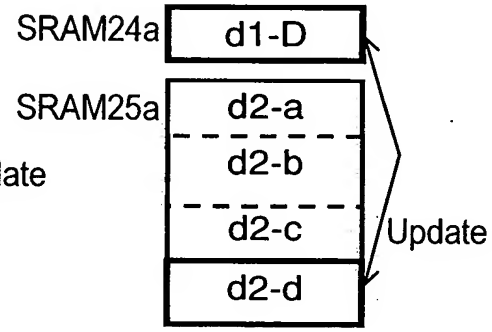


FIG. 7E



Reference marks in the drawings

21 LSI
22 ROM access control circuit
23 Flush ROM
24a、25a SRAMs
26 Video signal output circuit
27c Input/output terminal
28、29 Buffers
31 Selector
32 I/O control unit